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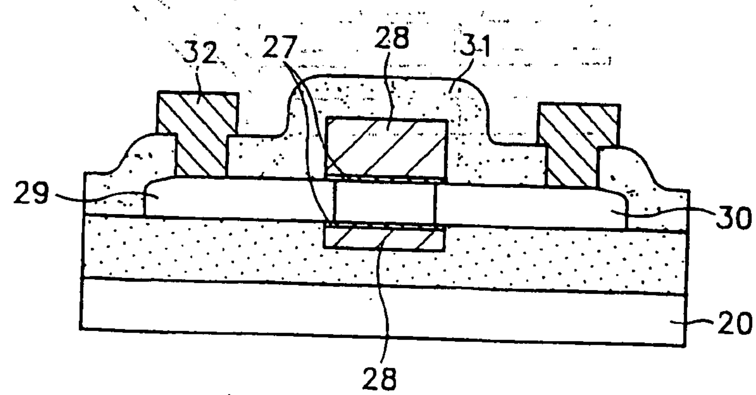
(54) **Method of manufacturing a silicon-on-insulator semiconductor device.**

(57) The present invention discloses a method for making a semiconductor device of silicon-on-insulator structure comprises the steps of: forming a pad oxide on a wafer including a lower silicon substrate, a buried oxide layer and an upper silicon layer, and forming an oxynitride region on a predetermined portion of the buried oxide layer; forming an active silicon layer to intersect the oxynitride region, and forming a cavity by wet-etching the exposed oxynitride region; forming a gate insulating layer on the surface of the exposed active silicon layer; forming a polysilicon to fill the cavity surrounding said active silicon layer and removing a predetermined portion of the doped polysilicon to form a gate electrode; and forming source and drain regions on the active silicon layer separated by the gate electrode.

FIG:9B



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The present invention relates to a method for making a semiconductor device in a silicon semiconductor well surrounded by an insulating layer by means of silicon-on-insulator techniques.

There produce active parasitic devices such as parasitic metal oxide semiconductor transistors or parasitic bipolar transistors in a PN junction separation structure that appears in a complementary metal oxide semiconductor structure. In addition, there are problems of deterioration of electric devices and soft error due to latch-up phenomenon. In order to prevent these problems and attain high density, there have been studied silicon-on-insulator (SOI) techniques that insulating layers are formed as sidewalls of an insulating substrate formed of a material such as SiO_2 and silicon single crystalline wells are formed in these insulating layers to form semiconductor devices in the above wells.

These techniques have advantages of perfect isolation of electrical elements, high speed performance, latch-up free and soft error free. That is, a semiconductor device such as CMOS circuits can be made. Second, the width of insulating layers for isolation depends on just photo-etching, etc. Third, high integration based on the micro-miniaturization can be obtained as well as the application with three-dimensional devices. According to the above techniques, a semiconductor device of SOI structure is formed by forming an amorphous or polysilicon layer on an amorphous insulating substrate such as SiO_2 and performing recrystallization on the polysilicon layer. Separation by implanted oxygen (SIMOX) processes, full isolation by phorous oxidized silicon (FIPOS) processes, or zone melting recrystallization (ZMR) are also known as another approach.

Recently, SOI MOSFET formed on a ultra-thin film of less than 1000 angstroms may be obtained, which has an effect to removal of kink and improvement of sub-threshold characteristic curve.

In addition to this, study has been made in the manufacture of SOI Gate-All-Around MOSFET structure. When a lower part of a hook-shape gate is formed underneath an active silicon region, in order to form an SOI wafer, a channel length of the lower part is dependent on a channel width region to be larger than the lower part of the channel width by isotropic wet etching, and the thickness of a buried oxide layer is more than half of the lower part of the channel width region. Accordingly, there is a limit to increasing the channel width region. If the thickness of the buried oxide layer of the SOI wafer is increased, energy and dose of oxygen ion implantation is remarkably increased, and defects are generated in the active silicon region to degrade the electrical characteristics.

In accordance with the present invention, there are made a perfect separation implanted oxygen (SIMOX) wafer and a partial separation implanted nitrogen (SIMNI) wafer, and by forming a buried oxide layer and an oxynitride layer included in the buried oxide layer and partially buried and making devices by selective etching, a channel length region is formed to be independent to a channel width or a thickness of the buried oxide layer.

It is an object of the present invention to provide a silicon-on-insulator metal oxide semiconductor field effect transistor (SOI MOSFET).

According to the present invention, a method for making a semiconductor device of silicon-on-insulator structure comprises the steps of:

forming a pad oxide on a wafer including a lower silicon substrate, a buried oxide layer or a buried nitride layer, and an upper silicon layer, and forming an oxynitride region on a predetermined portion of the buried oxide layer;

forming an active silicon layer to intersect the oxynitride region, and forming a cavity by wet-etching the exposed oxynitride region;

forming a gate insulating layer on the surface of the exposed active silicon layer;

forming a polysilicon to fill the cavity surrounding said active silicon layer and removing a predetermined portion of the doped polysilicon to form a gate electrode; and

forming source and drain regions on the active silicon layer separated by the gate electrode.

FIGS. 1A to 5C are the steps in the manufacture of a conventional silicon oxide insulator metal oxide semiconductor field effect transistor (SOI MOSFET);

FIGS. 6A to 9C are the steps in the manufacture of a silicon oxide insulator metal oxide semiconductor field effect transistor (SOI MOSFET) in accordance with the present invention; and

FIG. 10 is a perspective view of the structure of the SOI MOSFET.

In order to describe the present invention, making a silicon-on-insulator gate-all-around (SOI GAA) metal oxide semiconductor field effect transistor (MOSFET) is now described in detail, which is based on "SILICON-ON-INSULATOR "GATE-ALL-AROUND DEVICE" in pp 595 - 598 of IEDM written by J.P. Colinge and published on 1990.

First, there is prepared a separation implanted oxygen silicon-on-insulator (SIMOX SOI) wafer having a buried oxide layer 2 and an upper silicon layer 3 on a lower silicon substrate.

A pad oxide layer and a silicon oxide layer are formed over all the upper silicon layer 3, and a pattern having a section as shown in FIG. 2 through photo-etching processes, is formed.

The patterned upper silicon layer now becomes an active region 6, and the pad oxide layer 4 and silicon

nitride layer 5 are remained on top of the active region 6. And the silicon layer of side walls of the active region is exposed and thermally oxidized to form a thermal oxide layer 7 thereby surrounding the active region by insulating layers.

The side walls of the active region is thermally oxidized and squarish parts of the active region 6 is made round. By making round the edges where each side of the channels meets together not to produce high electric field, causes that degrade electrical characteristics such as leakage current or deterioration of the gate oxide layer may be minimized or removed.

Referring now to FIG. 2, the silicon nitride layer 5 is etched to be removed and a gate electrode is formed through photo-etching processes. The shape of the active region corresponds to a rectangular-form region designated by "A" in FIG. 3A.

The pattern of FIG. 3A is a pattern of photoresist 8, and is disposed on the substrate of FIG. 2. An opened region of a region "B" is to be etched. A region "C" is larger than the region, because of undercut by wet-etching with hydrofluoric solution. FIG. 3B is a sectional view as taken along line a-a' of FIG. 3A. FIG. 3C is a sectional view as taken along line b-b', and there is formed a cavity 9 that penetrates around the center of the active region 6 by undercutting by wet-etching. At this point, the nitride layer is etched, and the oxide layers surrounding the active region are removed to expose the pad oxide layer 2.

The photoresist 8 is removed after the steps in FIGS. 3A to 3C, and a gate oxide layer is formed on the surface of the active region 6, as shown in FIG. 4B. A size of "L_r" around the active region in FIG. 3A is a region where the silicon layer is exposed even in the active region, and an oxide layer 10B is formed as large as the size of "L_r" in FIG. 4B. The gate oxide layer is formed in such a manner, and ion implantation and annealing are performed to regulate a threshold voltage V_t. A polysilicon layer 11 is formed to fill the cavity, and the side surfaces and top of the active silicon region 6 are covered thereby.

FIG. 4A is a plan view of the resultant structure after the polysilicon layer has been formed, and FIGS. 4B and 4C are respectively sectional views as taken along lines a-a' and b-b'.

As shown in FIG. 5B, the polysilicon layer 11 of FIG. 4B is patterned to form a gate electrode 12 by photo-etching. The pattern of the photoresist layer is shown in FIG. 5A. A region indicated by "G" in FIG. 5A is a gate electrode pattern, and the gate electrode 12 is formed by the dry-etching. FIGS. 5B and 5C are respectively sectional views as taken along lines a-a' and b-b'. Ion implantation and drive-in processes are performed after the photoresist layer is removed, and source and drain regions 13, 14 are formed. An interlayer insulating layer 15 is coated, and photo-masking and opening for contact hole and removal of photoresist are performed. A first metal is deposited, and a first metal photo-masking, a first metal-etching, and removal of photoresist layer are performed to form a first metal line 16.

If a gate voltage V_G is applied in this SOI GAA structure MOSFET, a reverse layer is formed around the surface of the gate of the active silicon region 6. If a drain voltage V_D is applied between the source and drain regions, a channel current I_D flows. The channel current I_D is expressed as the following equation 1:

$$I_D = \frac{-Q_n W \mu V_D}{L} \quad (1)$$

The letters appearing in the equation (1) designate the followings: a channel width W; mobility μ; a channel length L; and a conductive electric charge per unit area Q_n. Channel transition time T_{tr} is proportional to the channel length, and inversely proportional to mobility and drain voltage, which is expressed as the following equation (2):

$$T_{tr} = \frac{L^2}{\mu V_D} \quad (2)$$

The channel drain electrode current I_D is proportional to conductive electric charge amount within the reverse layer, and inversely proportional to the channel transition time T_{tr}, which is expressed as the following equation (3):

$$I_D = \frac{-Q_N}{T_{tr}} \quad (3)$$

Accordingly, since the channel width/length (W/L) increases in the above equations (1) to (3), the channel drain electrode current I_D may be increased, and the channel length may be reduced so that the channel transition time T_{tr} may be reduced.

However, the above discussion is totally theoretical, and does not come true according to practical processes. Its reason will be described.

A cavity 9 is formed by means of undercutting according to wet-etching when etching process is performed to form a gate underneath the active silicon region of SOI GAA structure MOSFET. The channel length Lr, however, is actually larger than the channel width W_u of the lower part of the gate, as shown in FIG. 3A. This results from L_{ove} amount according to reasons of variation of L_p by excessive etching at the time of wet-etching

because there is a restriction to maintaining L_p width, a limit of photo-etching. In addition, the wet-etching acts as an isotropic tching. That is, Lr is appeared as $L_p + W_u + L_{ove}$. Besides the real channel width W_r is made by adding upper and lower portions and both side surfaces of the channel, and becomes $2(W_u + W_s)$. Strictly, there is a corner effect of W_s where W_u and W_{up} meets, which is not considered for convenience's sake.

The active silicon region in FIG. 3C is formed to be silicon island-like, and must be wet-etched as large as $1/2W_u$ in order that the channel penetrates crossing the silicon island under the silicon island. If wet-etching is performed, the buried oxide layer 2 is etched in the lengthwise direction of the silicon, i.e. toward the channel length from the surface as well as the silicon substrate from the surface. As a result, the silicon island should be etched as large as $1/2W_u$ in order that the channel penetrates when a distance where the channel penetrates the silicon island vertically is W_u, i.e. when the channel width under the silicon island is W_u, which should be considered regarding the channel length, since the etching is performed excessively in fact.

Besides, the width of the opened region by the gate photo-masking is added to formation of the whole channel length. The channel length L_r is increased as the channel width W_u becomes large.

If the thickness of the buried oxide layer is smaller than $1/2W_u$, the oxide layer is totally etched to expose the silicon substrate. And when the gate oxide layer is formed, the buried oxide layer is oxidized to be an insulated oxide layer having the thickness of the gate oxide layer between the gate lower electrode and the silicon substrate. Thus, the buried oxide layer serves as a capacitive oxide layer between the gate polysilicon and silicon substrate.

L_r/W_r value is one of the important factors determining the electrical characteristics of the device in MOSFET. The smaller the L_r/W_r value is, the more the ID value is increased. The transition time T_{tr} may be reduced such that the performance speed of the device is improved. In the above MOSFET, L_r/W_r becomes $(L_p + W_u + L_{ove})/2(W_u + W_s)$, and L_r and W_r depends on W_u in a great deal. As a result, if the channel width W_u is increased, L_r and W_r are increased simultaneously, and I_D and T_{tr} are not improved. Besides, the thickness of the buried oxide layer is increased according to the increase of the W_u value in order to reduce capacitive effect between the gate polysilicon and silicon substrate. Since the thickness of the buried oxide layer should be larger than $W_u/2 + L_{ove}$, energy and dose of the oxygen ion implantation should be increased at the time of making an SIMOX wafer. Accordingly, high density defects may be caused in the lower channel region of the active silicon region and the production cost is increased.

In the present invention, a partial SIMNI (separation implanted nitrogen) and a whole SIMOX wafer are made by oxygen ion implantation overall the surface and nitride ion implantation just over the lower gate at the time of making an SOI wafer, and the buried oxide layer is formed. And then, by forming a partial oxynitride layer between the upper silicon region and buried oxide layer, oxynitride of the oxynitride and oxide layer is selectively etched in H_3PO_4 solution to form the lower gate region, so as to solve the above problems.

The real channel length L_r' may be formed without regard to the real channel length W_r', and the I_D value and T_{tr} value may be improved thereby making a high performance SOI MOSFET.

The method for making an SOI MOSFET of the present invention is now described.

A pad oxide layer 24 is formed on a silicon substrate 20 as shown in FIG. 6A, and oxygen ion implantation is performed overall the surface. Nitride ion implantation is performed by an opened photoresist layer of a selected region corresponding to a position where a gate is formed underneath the active silicon to form an oxynitride region as indicated by "22" of FIGS. 6A and 6B. After the ion implantation is performed by means of a pattern of the photoresist layer "PR" of FIG. 6B, the used photoresist layer is removed. Annealing is carried out by ion implantation, and the silicon substrate 20, a buried oxide layer 21, an oxynitride region 22 and an upper silicon region 23 are formed. In order to form an active silicon region, the pad oxide layer 24 and upper silicon layer 23 are patterned by photo-etching to form a section as shown in FIG. 7B. FIG. 7A is a plan view of the substrate, and FIGS. 7B and 7C are respectively sectional views as taken along lines a-a' and b-b' of FIG. 7A. A region "A" is a patterned upper silicon layer 25, and a region "B" is the oxynitride region 22. A region "C" is the surface of the buried oxide layer 21 of FIG. 6. FIG. 7D is a perspective view thereof.

The PR layer of FIG. 7D is removed, and the oxynitride layer partially opened is undercut-etched by wet-etching method, and the pad oxide layer is also removed. The width of the oxynitride layer is determined by the opened region of the PR layer formed by photo-masking in FIG. 6B. Even if the length of the PR layer that is etched at the time of undercut-etching the oxynitride layer is long, etching the oxynitride layer is more speedly than etching an oxide layer, and the excessive etching hardly occurs in the lengthwise direction of the channel.

A part of the oxynitride layer is removed to be a cavity, and the pad oxide layer is etched by the same etching solution. The oxynitride is completely removed 100 times compared with the oxide.

A gate oxide layer 26 is formed by thermal oxidation on the exposed active silicon region 25. As shown in FIG. 8D, each of gate oxide layers 26A, 26B is formed on both the upper and lower portions of the silicon layer 25. Ion implantation is performed to regulate threshold voltage V_T. A polysilicon layer 27B is deposited to fill the cavity. A polysilicon 27A is formed on the surface of the substrate. FIG. 8A is a plan view of the sub-

strate on which the above processes are performed, and FIGS. 8B and 8C are sectional views as respectively taken along lines a-a' and b-b'.

Referring now to FIGS. 8A, 8B, 8C and 8D, the polysilicon layer 27A is patterned, and the gate electrode 28 is formed by photo-etching, as shown in FIG. 9B.

The size of the gate electrode corresponds to a region D, and after the formation of the gate electrode 28, ion implantation and drive-in processes are carried out so that source and drain regions 29, 30 are formed.

An interlayer insulating layer 31 and a first metal line 32 are formed to manufacture an SOI MOSFET of the present invention. FIG. 10 is a perspective view of the device before the interlayer insulating layer is formed, and the operation principle of the present invention is basically the same as the conventional SOI GAA structure MOSFET. In the manufacture of the conventional device, there is a problem in the improvement of electrical characteristics of MOSFET according to the value of L_r/W_r. Since values of the real channel length L_r' and the real channel width W_r' are formed to be independent of each other, the present invention has more effects to improvement of the electrical characteristics than the conventional device has. Besides, since the thickness of the buried oxide layer has nothing to do with the channel width, defects may be minimized at the time of the manufacture of an SOI wafer, and production cost can be saved.

L_r'/W_r' may be expressed as the following equation (4):

$$\frac{L_r'}{W_r'} = \frac{(L_p + Ldiff + L_{ove}')}{2(W_u + W_s)} \quad (4)$$

L_{diff} is a channel length extended at the time of nitride ion implantation and annealing, and Love' has a value of almost zero by high selection ratio L_r' is dominant than L_p in FIG. 8B.

A semiconductor memory device is a memory unit cell and has a metal oxide semiconductor (MOS) device and a capacitance. The SOI MOSFET may be used as the one MOS device. The channel length/width is determined as follows, according to the design rule of 256 M bit capacitance:

Example 1: If $L_p = 0.25\mu m$, $L_{diff} = 0.1\mu m$,
$W_u = 0.25\mu m$, $W_s = 0.2\mu m$,
$L_{ove} = 0.1 \times W_u - 0.025$, and $L_{ove}' = 0$,
$L_r/W_r = 0.58$, $L_r'/W_r' = 0.39$

Example 2: If $L_p = 0.6\mu m$, $L_{diff} = 0.2\mu m$, $W_u = 20\mu m$,
$W_s = 0.2\mu m$, $L_{ove} = 0.1\mu m$, and $L_{ove}' = 0$,
$L_r/W_r = 0.51$, $L_r'/W_r' = 0.019$

In the above examples, since W_r equals to W_r', L_r' has a value smaller than L_r, and better effect of the electrical characteristics may be requested.

If the conventional method is used in the example 2, the thickness of the buried oxide layer is the same as the thickness of the gate oxide layer between the lower gate and silicon substrate, which may serve as. a capacitor according to the difference of voltage applied between the gate and silicon substrate.

This may be a factor of degradation of the electrical elements and occurance of leakage current I_{sub} by breakdown. If the thickness of the buried oxide layer is fully removed, e.g. about 1μm, W_u cannot be used more than about 2μm.

The manufacturing steps in FIGS. 6A to 10 propose examples of concrete numerical values. The p-type silicon substrate is used, and the oxide layer is formed to a thickness of 500 angstroms. Oxygen ions implanted thereto is 10^{18} atoms/cm², 180 KeV, and nitride ions are implanted at 7.5×10^{17} atoms/cm², 140KeV to form the oxynitride region 22. Annealing by ion implantation is performed for two hours at 1200°C. The etching thickness of the pad oxide layer and active silicon region are 500 angstroms and 2000 angstroms, respectively. Undercut-etching of the oxynitride is performed in H_3PO_4 at 170°C, and etching the pad oxide layer is to a thickness of 500 angstroms. The thickness of the gate oxide layer is 240 angstroms and boron ions are implanted at 10^{13} atoms/cm², 60 KeV. The condition of the drive-in process is 900°C, 30 min. in an ambient of N_2.

The thickness of the deposited polysilicon is 3000 angstroms, and As ions are implanted at 7×10^{15}, 100 KeV. Source and drain regions are formed by drive-in process for thirty minutes at 900°C. As an interlayer insulating layer, the oxide layer has a thickness of 6000 angstroms, and a first metal is formed to a thickness of 6000 angstroms to form the device.

According to the conventional SOI GAA structure MOSFET, the channel length L_r and thickness of the buried oxide layer are always dependent on the channel width, and L_r/W_r cannot be small.

If the upper and lower portions of the channel width are increased, since the SOI wafer is manufactured with just the thin oxide layer between the silicon substrate and gate, such a structure becomes a factor of occurance of leakage current by deterioration to insulation of the oxide layer.

In the present invention, however, since the channel length and the thickness of the buried oxide layer may be formed independently of the channel width, L_r'/W_r' value may be very small to obtain the improved

electric characteristics of the device.

Claims

1. A method for making a semiconductor device of silicon-on-insulator structure comprising the steps of:
   forming a pad oxide on a wafer including a lower silicon substrate, a buried oxide layer or a buried nitride layer, and an upper silicon layer, and forming an oxynitride region on a predetermined portion of said buried oxide layer;
   forming an active silicon layer to intersect said oxynitride region, and forming a cavity by wet-etching said exposed oxynitride region;
   forming a gate insulating layer on the surface of the exposed active silicon layer;
   forming a polysilicon to fill said cavity surrounding said active silicon layer and removing a predetermined portion of said doped polysilicon to form a gate electrode; and
   forming source and drain regions on said active silicon layer separated by said gate electrode.

2. The method according to claim 1, wherein said oxynitride region is formed by nitride ion-implantation.

FIG. 1 (Prior Art)

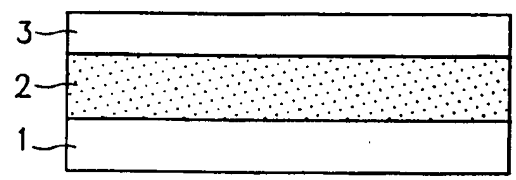


FIG. 2 (Prior Art)

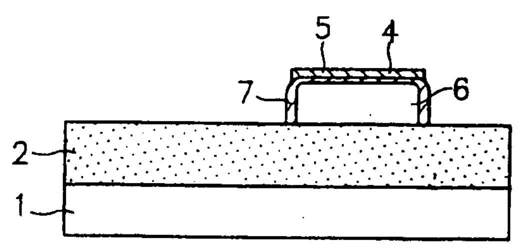


FIG.3A (Prior Art)

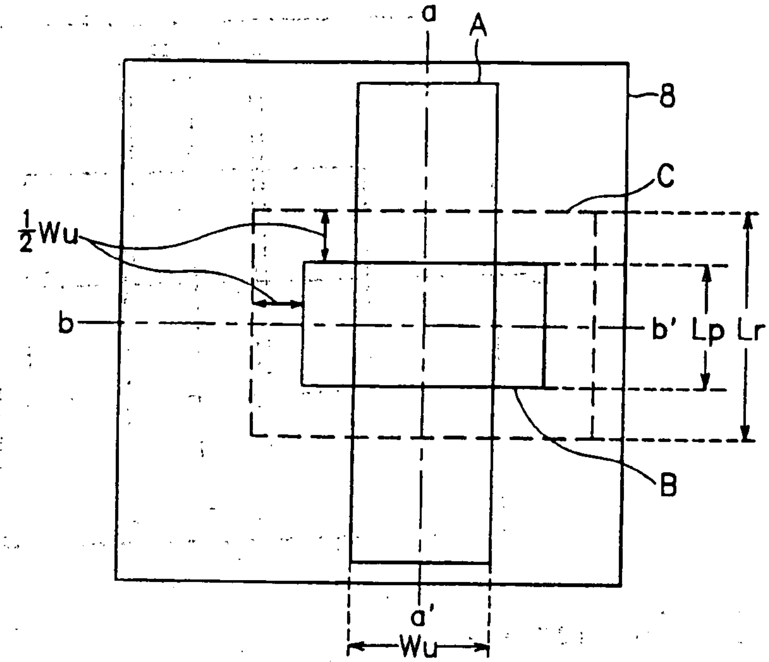


FIG.3B (Prior Art)

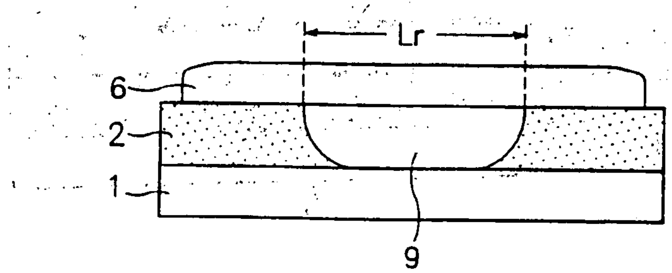


FIG.3C (Prior Art)

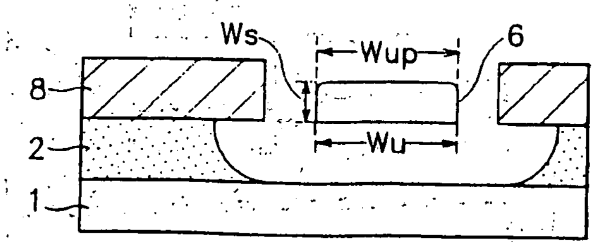


FIG.4A(Prior Art)

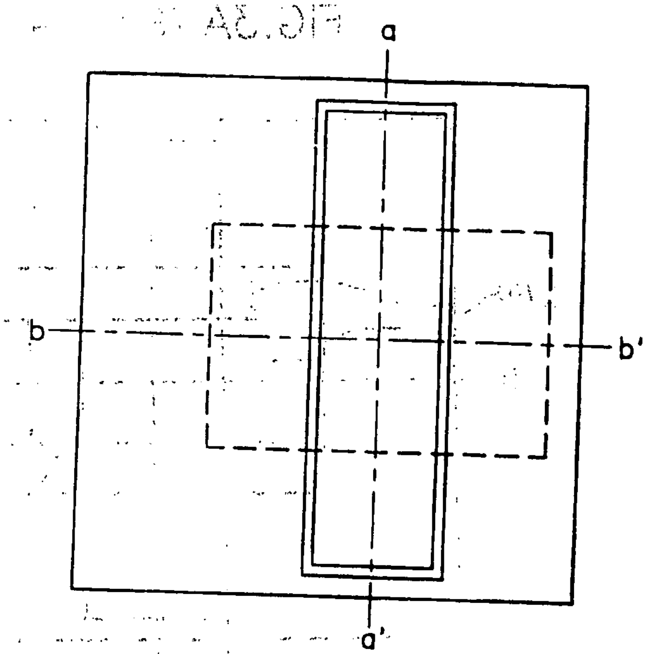


FIG.4B(Prior Art)

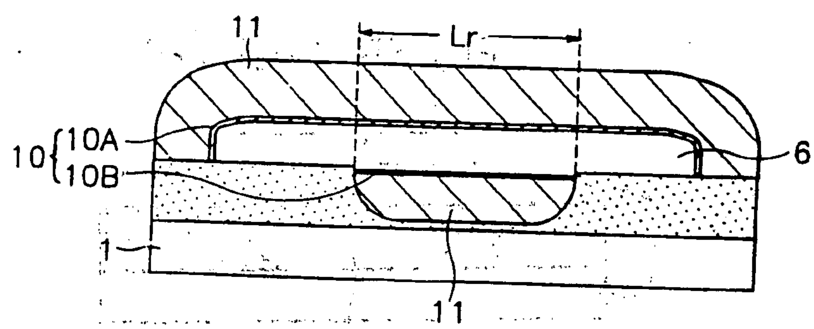


FIG.4C(Prior Art)

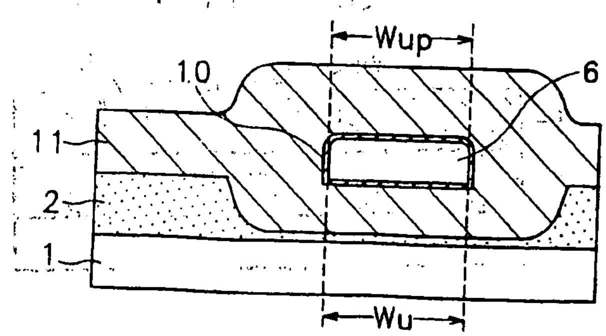


FIG.5A (Prior Art)

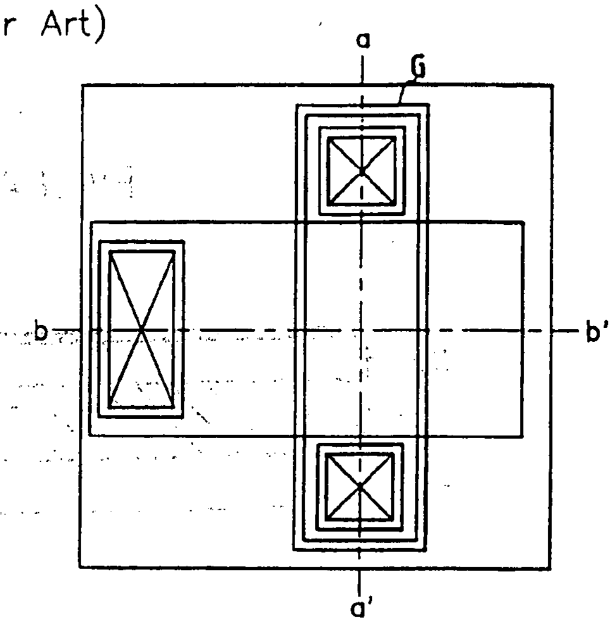


FIG.5B (Prior Art)

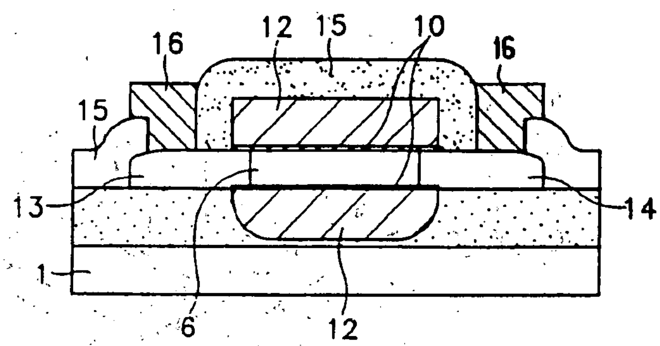


FIG.5C (Prior Art)

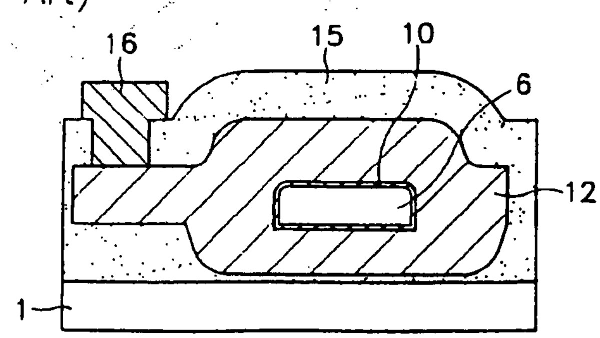


FIG.6A

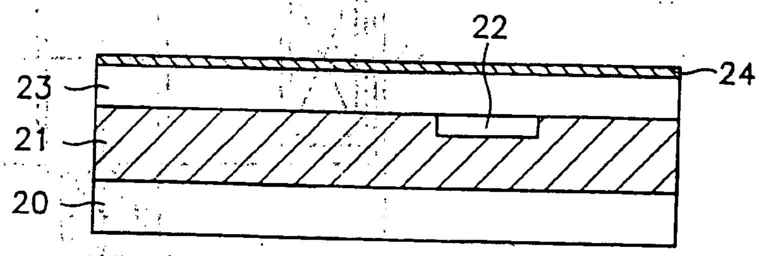


FIG.6B

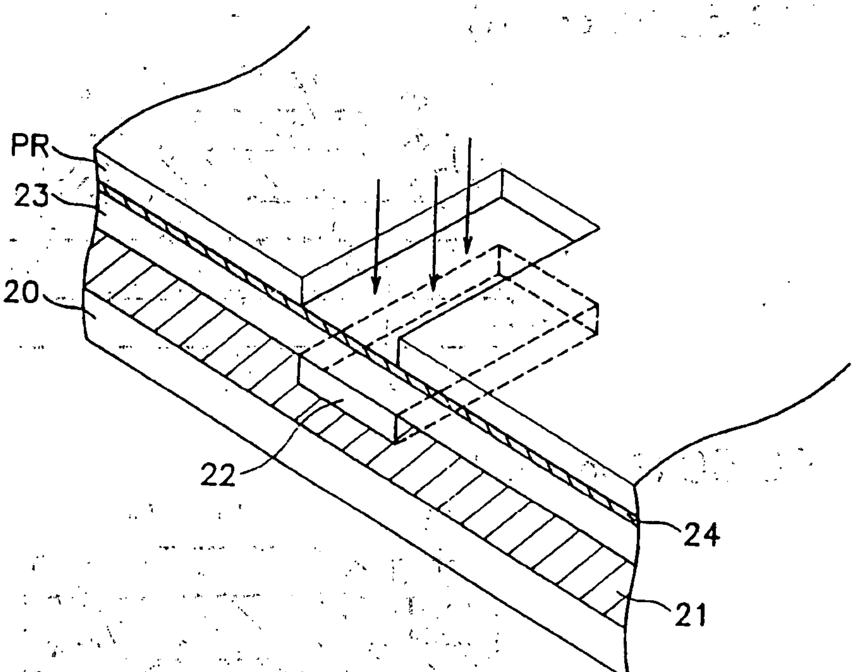


FIG.7A

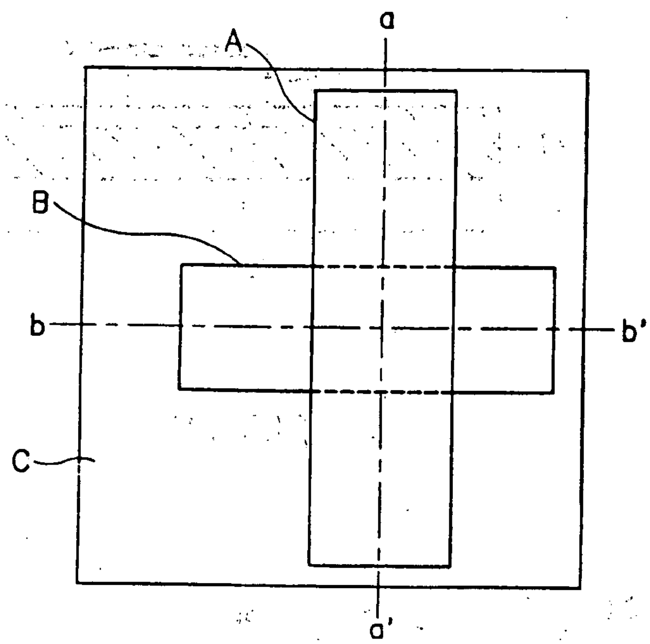


FIG.7B

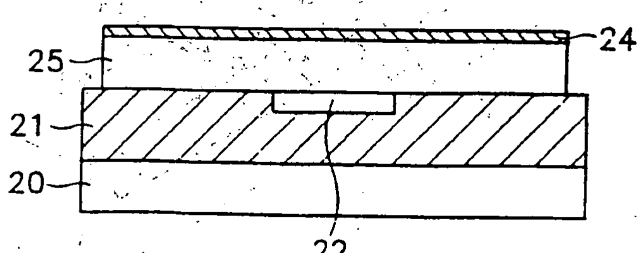


FIG.7C

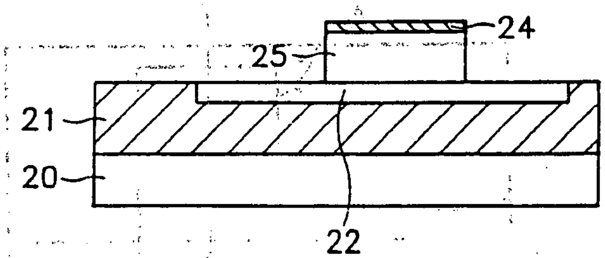


FIG.7D

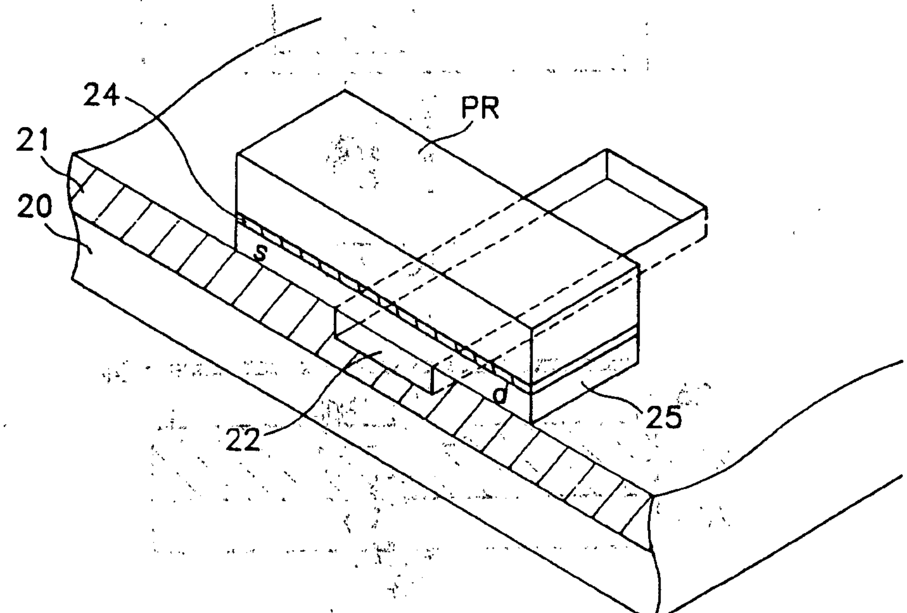


FIG.8A

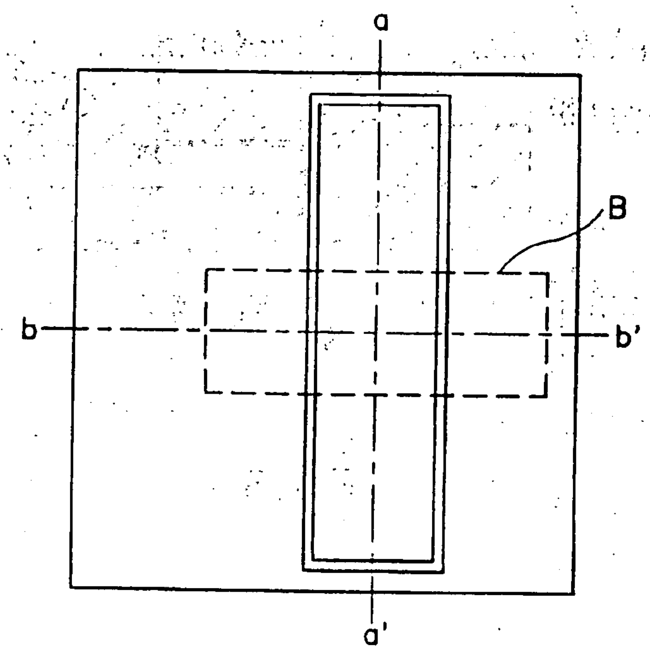


FIG.8B

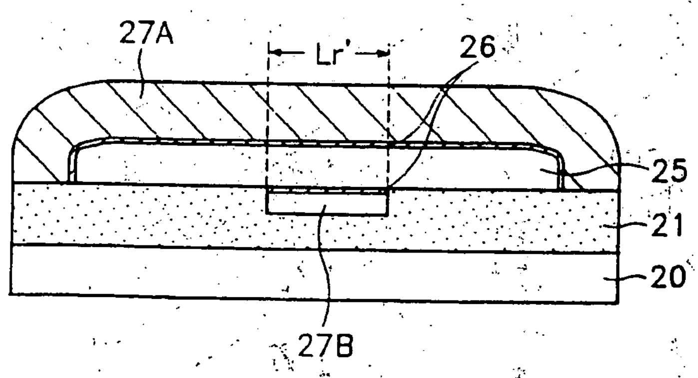


FIG.8C

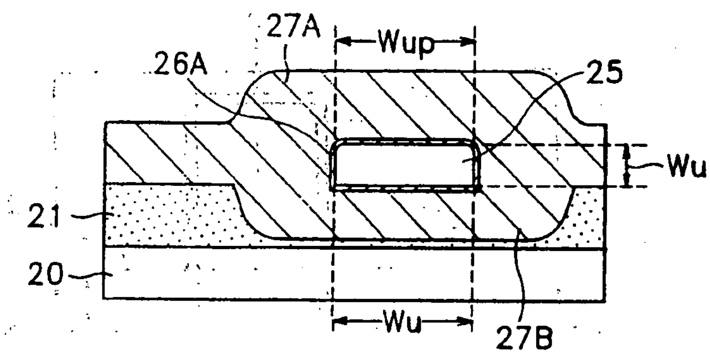


FIG.8D

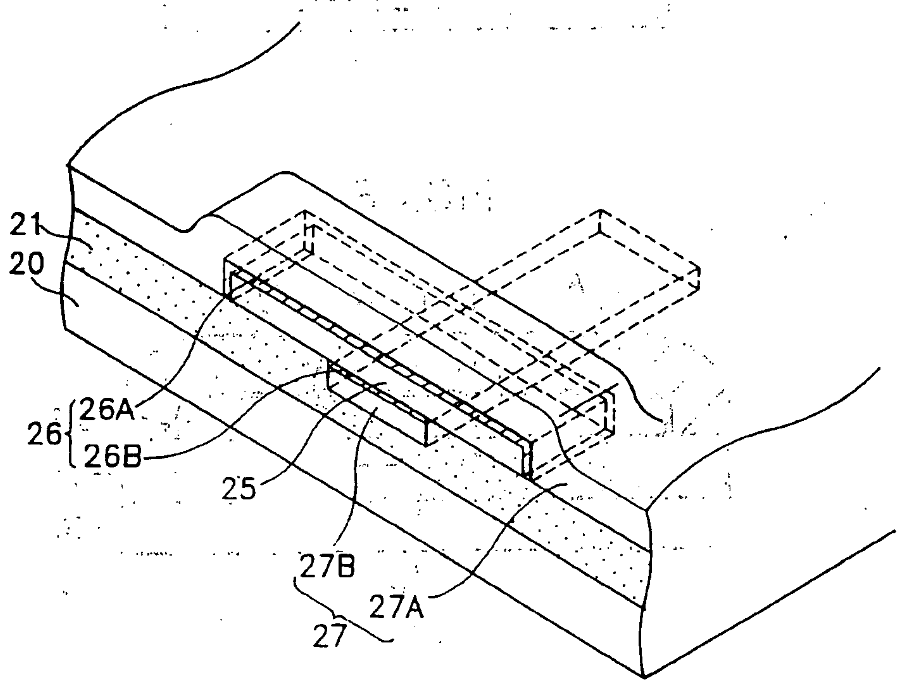


FIG. 9A

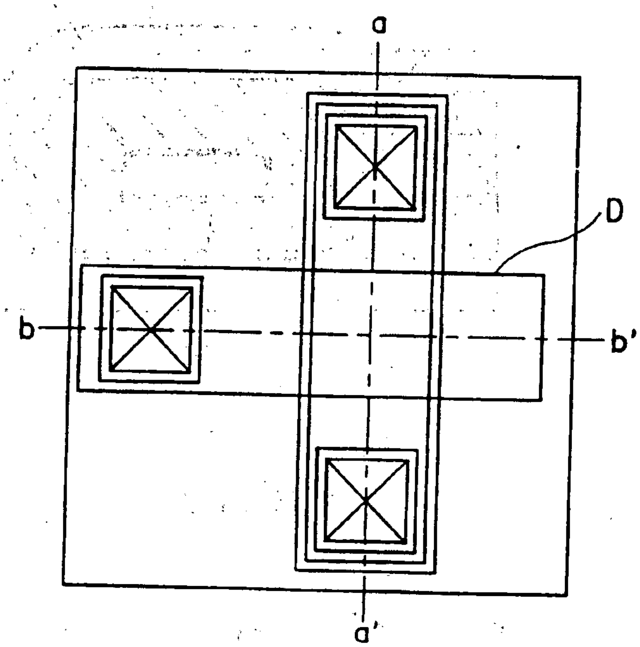


FIG. 9B

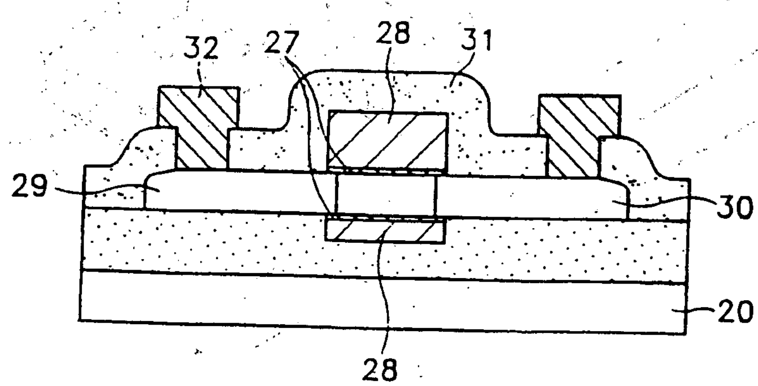


FIG.9C

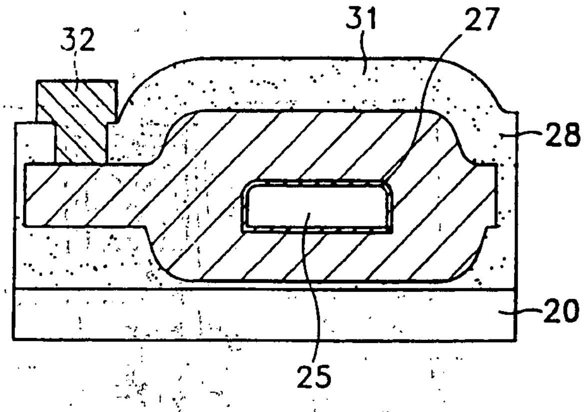
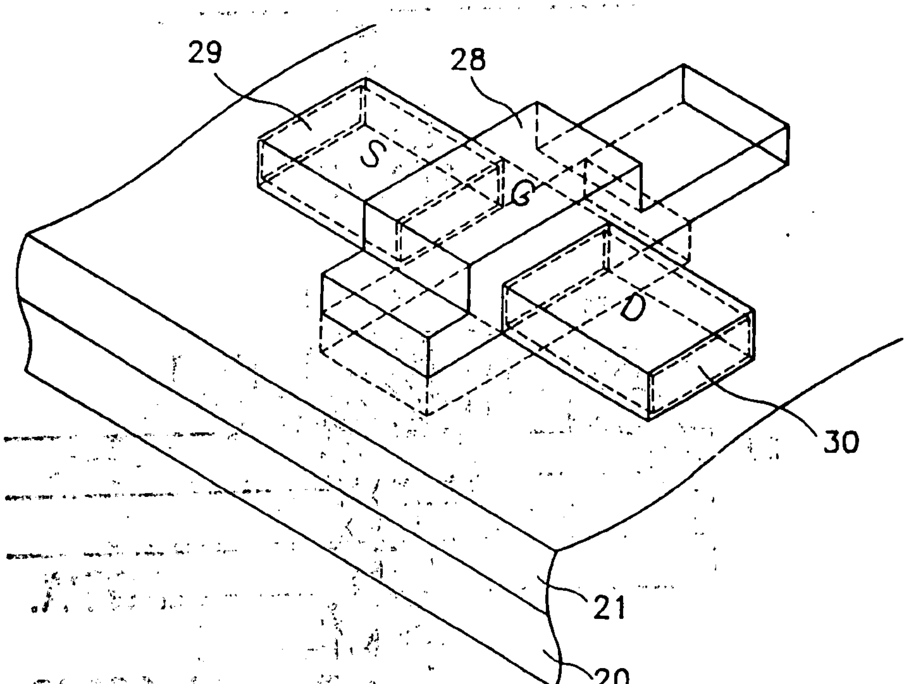


FIG.10



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